
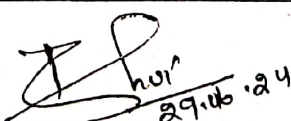


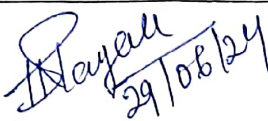
# ACADEMIC SESSION : 2024-25

Discipline : Electrical Engineering	Semester : 5 <sup>th</sup>	Name of the Teaching Faculty : Tilu Behera
Subject : Digital Electronics & Microprocessor	No. of days / week class allotted : 5	Semester From date: 01-07-2024 to 08-11-2024 Nos. of Weeks per semester : 15
Week	Class Day	Theory/ Practical Topics
1 <sup>ST</sup>	1 <sup>st</sup>	Binary, Octal, Hexadecimal number systems
	2 <sup>nd</sup>	Compare Binary, Octal, Hexadecimal number systems with Decimal system
	3 <sup>rd</sup>	Binary addition, subtraction
	4 <sup>th</sup>	Binary Multiplication and Division.
	5 <sup>th</sup>	1's complement and 2's complement numbers for a binary number
2 <sup>ND</sup>	1 <sup>st</sup>	Subtraction of binary numbers in 2's complement method.
	2 <sup>nd</sup>	Use of weighted and Un-weighted codes
	3 <sup>rd</sup>	write Binary equivalent number for a number in 8421, Excess-3 and Gray Code and vice-versa.
	4 <sup>th</sup>	Importance of parity Bit.
	5 <sup>th</sup>	Logic Gates: AND, OR, NOT, NAND, NOR and EX-OR gates with truth table.
3 <sup>RD</sup>	1 <sup>st</sup>	Realize AND, OR, NOT operations using NAND, NOR gates.
	2 <sup>nd</sup>	Different postulates and De-Morgan's theorems in Boolean algebra.
	3 <sup>rd</sup>	Use Of Boolean Algebra For Simplification Of Logic Expression
	4 <sup>th</sup>	Karnaugh Map For 2,3,4 Variable
	5 <sup>th</sup>	Simplification Of SOP And POS Logic Expression Using K-Map
4 <sup>TH</sup>	1 <sup>st</sup>	Give the concept of combinational logic circuits
	2 <sup>nd</sup>	Half adder circuit and verify its functionality using truth table.
	3 <sup>rd</sup>	Realize a Half-adder using NAND gates only and NOR gates only.
	4 <sup>th</sup>	Full adder circuit and explain its operation with truth table.
	5 <sup>th</sup>	Realize full-adder using two Half-adders and an OR – gate and write truth table
5 <sup>TH</sup>	1 <sup>st</sup>	Full subtractor circuit and explain its operation with truth table.
	2 <sup>nd</sup>	Operation of 4 X 1 Multiplexers
	3 <sup>rd</sup>	Operation of 1 X 4 Demultiplexer
	4 <sup>th</sup>	Working of Binary-Decimal Encoder
	5 <sup>th</sup>	Working of 3 X 8 Decoder.
6 <sup>TH</sup>	1 <sup>st</sup>	Working of Two bit magnitude comparator.
	2 <sup>nd</sup>	Give the idea of Sequential logic circuits.
	3 <sup>rd</sup>	State the necessity of clock and give the concept of level clocking and edge triggering.
	4 <sup>th</sup>	Clocked SR flip flop with preset and clear inputs.
	5 <sup>th</sup>	Construct level clocked JK flip flop using S-R flip-flop and explain with truth table
7 <sup>TH</sup>	1 <sup>st</sup>	Concept of race around condition and study of master slave JK flip flop.
	2 <sup>nd</sup>	Give the truth table of edge triggered D flip flop and draw it's symbol.
	3 <sup>rd</sup>	Give the truth table of edge triggered T flip flop and draw it's symbol.
	4 <sup>th</sup>	Applications of flip flops.
	5 <sup>th</sup>	Define modulus of a counter

8 <sup>TH</sup>	1 <sup>st</sup>	3-bit asynchronous counter and its timing diagram.
	2 <sup>nd</sup>	4-bit asynchronous counter and its timing diagram.
	3 <sup>rd</sup>	Asynchronous decade counter.
	4 <sup>th</sup>	4-bit synchronous counter
	5 <sup>th</sup>	Distinguish between synchronous and asynchronous counters.
9 <sup>TH</sup>	1 <sup>st</sup>	State the need for a Register and list the four types of registers.
	2 <sup>nd</sup>	Working of SISO Register with truth table using flip flop.
	3 <sup>rd</sup>	Working of SIPO Register with truth table using flip flop.
	4 <sup>th</sup>	Working of PISO Register with truth table using flip flop.
	5 <sup>th</sup>	Working of PIPO Register with truth table using flip flop.
10 <sup>TH</sup>	1 <sup>st</sup>	Introduction to Microprocessors, Microcomputers
	2 <sup>nd</sup>	Architecture of Intel 8085A Microprocessor and description of each block.
	3 <sup>rd</sup>	Architecture of Intel 8085A Microprocessor and description of each block.
	4 <sup>th</sup>	Pin diagram and description.
	5 <sup>th</sup>	Pin diagram and description.
11 <sup>TH</sup>	1 <sup>st</sup>	Stack, Stack pointer & stack top
	2 <sup>nd</sup>	Interrupts
	3 <sup>rd</sup>	Opcode & Operand,
	4 <sup>th</sup>	Differentiate between one byte, two byte & three byte instruction with example.
	5 <sup>th</sup>	Instruction set of 8085 example
12 <sup>th</sup>	1 <sup>st</sup>	Instruction set of 8085 example
	2 <sup>nd</sup>	Addressing mode
	3 <sup>rd</sup>	Addressing mode
	4 <sup>th</sup>	Fetch Cycle, Machine Cycle, Instruction Cycle, T-State
	5 <sup>th</sup>	Timing Diagram for memory read, memory write
13 <sup>th</sup>	1 <sup>st</sup>	Timing Diagram for I/O read, I/O write
	2 <sup>nd</sup>	Timing Diagram for 8085 instruction
	3 <sup>rd</sup>	Problems on Timing Diagram for 8085 instruction
	4 <sup>th</sup>	Counter and time delay.
	5 <sup>th</sup>	Simple assembly language programming of 8085
14 <sup>th</sup>	1 <sup>st</sup>	Question Discussion
	2 <sup>nd</sup>	Question Discussion
	3 <sup>rd</sup>	Question Discussion
	4 <sup>th</sup>	Basic Interfacing Concepts, Memory mapping & I/O mapping
	5 <sup>th</sup>	Functional block diagram and description of each block of Programmable peripheral interface Intel 8255
15 <sup>th</sup>	1 <sup>st</sup>	Application using 8255: Seven segment LED display
	2 <sup>nd</sup>	Application using 8255: Square wave generator
	3 <sup>rd</sup>	Application using 8255: Traffic light Controller
	4 <sup>th</sup>	Question Discussion
	5 <sup>th</sup>	Question Discussion

  
 Prepared By  
 Tilu Behera  
 Lecturer in Electronics  
 GP Sonepur

  
 Head of the Department  
 Electrical Engineering  
 GP Sonepur

  
 Academic Coordinator  
 GP Sonepur